a source-drain wiring layer electrically connected to said source-drain region; and

a gate wiring layer electrically connected to said gate electrode.

REMARKS

Claims 25-36 and 38-60 are pending. By this Amendment, claim 26 is amended. Reconsideration based on the above amendments and following remarks is respectfully requested.

Applicants appreciate the Office Action's indication that claims 25, 39, 43, 44, 47-57, 59 and 60 are allowed.

The attached Appendix includes a marked-up copy of the rewritten claim (37 C.F.R. §1.121(c)(1)(ii)).

I. CLAIMS 27-29, 32, 45 AND 46 SATISFY THE REQUIREMENTS OF 35 U.S.C. §112, FIRST PARAGRAPH

The Office Action rejects claims 27-29, 32, 45 and 46 under 35 U.S.C. §112, first paragraph as containing subject matter not described in the specification. Applicants respectfully disagree with this assertion.

Regarding claims 27 and 28, each depending from claim 25, the Office Action asserts that the specification does not describe the gate electrode comprising an extension extending from both sides of the at least one part opposed to the channel region along a channel length direction and further comprising another extension extending from both ends (claim 27), r from at least one end (claim 28), respectively, of the gate electrode along a channel length direction. Applicants respectfully disagree with this assertion. Specifically, Figures 1, 2 and 5 show these features.

Regarding claims 27 and 28, each depending from claim 26, the Office Action asserts that the specification does not describe a thin film transistor comprising a channel region with an extension extending along both directions of the channel width and a gate electrode

comprising an extension extending from both ends (claim 27), or from at least one end (claim 28), respectively, of the gate electrode along a channel length direction. Applicants respectfully disagree with this assertion. Specifically, Figures 1, 3 and 5 show these features.

Regarding claim 29, the Office Action asserts that the specification does not describe the features of claim 28 and a gate wiring electrically connected to the at least one end of the gate electrode through a plurality of contact holes. Applicants respectfully disagree with this assertion. The features claimed in claim 29 are shown in Figures 1-5.

Regarding claim 32, the Office Action asserts that the specification does not describe the gate electrode comprising an extension extending from both sides of the at least one part opposed to the channel region along a channel length direction and further comprising a channel region including an extension extending along at least one direction of the channel width. Applicants respectfully disagree with this assertion. Specifically, Figure 3 discloses channel region 17 provided with extensions 171.

Regarding claim 45, the Office Action asserts that the specification does not describe a thin film transistor wherein at least one of the source or drain region and the gate electrode comprises an extension over which a plurality of contact holes are formed (as claimed in independent claim 44), and wherein the channel region includes an extension extending along both directions of the channel width (claim 45). Applicants respectfully disagree with this assertion. First, claim 44 has been allowed. Thus, all its features are described in the specification. Further, Figure 3 discloses channel region 17 provided with extensions 171.

Regarding claim 46, the Office Action asserts that the specification does not describe a thin film transistor wherein at least one of the source or drain region and the gate electrode comprises an extension over which a plurality of contact holes are formed (as claimed in independent claim 44), and wherein the gate electrode comprises an extension extending from both ends of the gate electrode along a channel length direction (claim 46). Applicants

respectfully disagree with this assertion. As stated above, claim 44 has been allowed. Thus, all its features are described in the specification. Further, Figures 1, 2 and 5 show these features.

Withdrawal of the rejection under 35 U.S.C. §112, first paragraph is respectfully requested.

II. THE CLAIMS DEFINE ALLOWABLE SUBJECT MATTER

The Office Action rejects claims 26, 30-31 and 33-34 under 35 U.S.C. §102(b) as anticipated by, or in the alternative, under 35 U.S.C. §103(a) as obvious over, U.S. Statutory Invention Registration H1435 to Cherne et al. (hereinafter "Cherne"); and rejects claims 35-36, 38, 40-42 and 58 under 35 U.S.C. §103(a) as obvious over Cherne in view of U.S. Patent No. 5,616,935 to Koyama et al (hereinafter "Koyama"). These rejections are respectfully traversed.

Cherne, either alone or in combination with Koyama, does not disclose, teach or suggest the claimed invention, as claimed in claims 26, 30-31, 32-36, 38 and 40-42.

Regarding independent claim 26, Cherne does not disclose, teach or suggest a thin film transistor comprising, inter alia, a silicon film in which a channel region is formed, the channel region including an extension in a channel width direction, and a gate electrode exhibiting higher thermal conductivity than that of the silicon film, the gate electrode formed over the channel region and covering up the extension, as claimed in independent claim 26.

Instead, Cherne, at col. 4, lines 17-34 and in Figs. 3 and 4, discloses a CMOS whose channel region 14 has protruded sections 31, 32. The purpose of the protruded sections 31, 32 is to reduce current leakage at the OFF state of the CMOS.

In contrast to Cherne, in the claimed invention, the extension in a channel width direction is arranged so as to suppress temperature rise in the channel region at ON state f the TFT.

Further, the recited feature of a gate electrode exhibiting higher thermal conductivity than that of the silicon film, as claimed in claim 26, enables the TFT to suppress the temperature rise of the channel region at ON state of the TFT because the heat generated in the channel region during the ON state can be radiated towards the gate electrode with higher thermal conductivity. Thus, the recited feature of a gate electrode exhibiting higher thermal conductivity is an important element to achieve the objective of radiating the heat generated in the channel region.

Moreover, the recited feature of the gate electrode covering up the extension, as claimed in claim 26, is also an important element to achieve the objective of radiating the heat generated in the channel region. Without being covered up by the gate electrode, the extension does not work as a radiator.

In contrast to the claimed invention, Cherne, at col. 4, line 21, discloses that a polysilicon, which is equivalent to the silicon film formed underneath thereof, is used as a gate electrode. Therefore, Cherne discloses that the thermal conductivity is the same between the gate electrode and the channel, and thus heat radiation from the channel to the gate electrode cannot be achieved. In Cherne, the protruded sections 31, 32 of the channel regi n never work as a heat radiator.

For at least these reasons, it is respectfully submitted that claims 26, 30-31 and 33-34 are distinguishable over the applied art. Withdrawal of the rejection under 35 U.S.C. §102(b) or 35 U.S.C. §103(a) is respectfully requested.

Regarding dependent claims 35, 36, 38, 40-42 and 58, Applicants submit that Koyama does not make up for the deficiencies of Cherne discussed above. Furthermore, Koyama provides no motivation for modifying its structure to match the claimed invention.

Thus, Applicants respectfully submit that, taken separately or together, Koyama and Cherne do not teach or suggest the present invention as claimed in claims 35, 36, 38, 40-42 and 58.

As required by MPEP Section 706.02(j), to establish a prima facie case of obviousness, these basic criteria must be met:

1) There must be some suggestion or motivation in the references themselves or in the knowledge generally available;

2) Reasonable expectation of success;

3) The prior art reference must teach or suggest all claim limitations.

The first and third requirements have not been met by the rejections of the Office Action. Neither Cherne nor Koyama show any motivation to modify the structure to achieve the claimed invention, and the Office Action clearly admits that there is an essential part of the claimed invention missing in Cherne.

For at least these reasons, it is respectfully submitted that claims 35, 36, 38, 40-42 and 58 are distinguishable over the applied art. Withdrawal of the rejection under 35 U.S.C. §103(a) is respectfully requested.

III. CONCLUSION

For at least the reasons discussed above, it is respectfully submitted that this application is in condition for allowance.

Should the Examiner believe that anything further is desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact Applicants' undersigned representative at the telephone number listed below.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

George P. Simion
Registration No. 47,089

JAO:GPS/hs

Attachments:
Appendix
Petition for Extension of Time

Date: December 9, 2002

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461

APPENDIX

Changes to Claims:

The following is a marked-up version of the amended claim 26:

26. (~~Twice~~ Thrice Amended) A thin film transistor comprising:

a silicon film in which a channel region is formed, the channel region ~~includes~~ including an extension ~~along both directions of~~ in a channel width direction;

a gate electrode exhibiting higher thermal conductivity than that of the silicon film, the gate electrode formed over the channel region and covering up the extension;

a gate insulating film provided between the channel region and the gate electrode; ~~and~~

a source-drain region connected to said channel region;

a source-drain wiring layer electrically connected to said source-drain region; and

a gate wiring layer electrically connected to said gate electrode~~,~~

~~wherein the channel region includes an extension extending along both directions of the channel width~~.